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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,868	06/26/2003	William J. Grundmann	884.A38US1	5510

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EXAMINER	
WHITMORE, STACY	
ART UNIT	**PAPER NUMBER**
2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/606,868	GRUNDMANN, WILLIAM J.	
	Examiner	Art Unit	
	Stacy A. Whitmore	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,8-11,15-17 and 21-23* is/are rejected.

7)☒ Claim(s) *4,6,7,12-14 and 18-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *6/26/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

FINAL ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-3, 5, 8-11, 15-17, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Vashi (US Patent 6,219,819).

2. As for claims 1-3, 5, 8-11, and 15-17, Vashi 6,219,819 discloses the invention as claimed, including a method, apparatus, and article of manufacture comprising machine accessible medium including instructions for adding bypass logic in a digital circuit design, wherein adding/creating comprises transforming a conditional state element into a logically redundant element in the digital circuit design, the transforming comprising:

[Note that the limitations " adding bypass logic in a digital circuit design", and transforming a conditional state element into a logically redundant element" in the preamble of the claim is not given patentable weight because the limitation has no bearing on the actual transformation steps in the body of the claim. Further, the limitation "adding bypass logic in a digital circuit design is accomplished by the transformation steps as rejected in the following claims]

Coupling a first latency delay unit to a data input of the conditional state element [fig. 3, elements 301-303 – first latency delay units, elements 321-323 – conditional state elements];

Coupling a second latency delay unit to an enable input of the conditional state element [fig. 3, elements 304-306 – second latency delay units, elements 321-323 – conditional state elements];

Coupling a first input of a multiplexer to an output of the conditional state element [fig. 3, elements 301-306 – multiplexers, elements 321-323 – conditional state elements, the first and second inputs of the multiplexers are coupled in several ways to the Q outputs of the elements 321-323];

Coupling a second input of the multiplexer to the data input of the conditional state element [fig. 3, elements 301-306 – multiplexers, elements 321-323 – conditional state elements, the first and second inputs of the multiplexers are coupled in several ways to the Q outputs of the elements 321-323];

Coupling a select line of the multiplexer to the enable input of the conditional state element [fig. 3, elements 301-306 – multiplexers, elements 321-323 – conditional state elements, the scan in/ enable inputs of the multiplexers are coupled in several ways to the Q outputs of the elements 321-323];

A memory, processor, bus coupled to the memory and processor, identifying a conditional state element [fig. 1, col. 4, lines 10-52];

Coupling first and second latency delay unit comprises a signal with a delay of one unit into the data input of the conditional state element [the signal from elements 301-306 have at least a delay of one unit];

Transforming any one of a flip-flop, register file, and a deterministic memory into a logically redundant element [fig. 3], the conditional state element comprises at least one of a flip-flop, register file, and a deterministic memory [fig. 3, elements 321-323].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject

matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vashi (US Patent 6,219,819) in view of McFarland (US Patent 6,212,629).

4. As for claims 22-23, Vashi discloses the invention as claimed, including the machine readable-medium that provides instructions for creating bypass logic in a digital circuit design that is without bypass logic, wherein creating comprises transforming a conditional state element into a logically redundant element as cited above.

Vashi does not specifically disclose replacing the conditional state element with a first multiplexer coupled to a first latency delay unit and coupling a second multiplexer that is coupled to a second latency delay unit to the first multiplexer.

McFarland discloses replacing conditional state element with a first multiplexer coupled to a first latency delay unit and second multiplexer that is coupled to a second latency delay unit to the first multiplexer [fig. 9C; col. 21 line 30 – col. 22, 10; wherein McFarland discloses that to replacement may be done between more than one pipeline stage, therefore incorporating a second multiplexer coupled to another delay unit as well as being coupled to the first multiplexer].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Vashi and McFarland because replacing Vashi's conditional state elements with multiplexers would have improved the handling of

latency delays in a pipelined architecture for improving the throughput of data [see McFarland, col. 21, line 64 – col. 22, line 7].

5. Applicant's arguments, filed December 1, 2006, with respect to claims 1-23 have been fully considered and are persuasive. The 35 USC 112 rejection of claims 1-23 has been withdrawn.

6. Applicant's arguments with respect to claims 1-3, 5, 8-11, 15-17, and 21-23 filed December 1, 2006 have been fully considered but they are not persuasive.

7. In the remarks, applicant argues in substance:

I. Vashi does not disclose where the limitation of "transforming of a conditional state element into a logically redundant element" is disclosed.

Examiner respectfully disagrees for the following reasons:

As to argument I: Vashi does disclose where the limitation of "transforming of a conditional state element into a logically redundant element" is disclosed [Note that the limitations " adding bypass logic in a digital circuit design", and transforming a conditional state element into a logically redundant element" in the preamble of the claim is not given patentable weight because the limitation has no bearing on the actual transformation steps in the body of the claim. Further, the limitation "adding bypass logic in a digital circuit design is accomplished by the transformation steps comprising a configuring of connection of elements]. Examiner specifically cited fig. 3 and col. 4, with respect to specific elements, especially in the rejection of claims 1-3, 5, 8-11, 15-17, and 21.

8. Claims 4, 6-7, 12-14, and 18-20 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to disclose either singularly or in combination the invention as claimed including the methods, apparatus, and computer readable medium where the claimed subject matter of the F and G functions is claimed.

10. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A. Whitmore whose telephone number is (571) 272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stacy A Whitmore
Primary Examiner
Art Unit 2825

SAW
February 12, 2007